High Speed VLSI Architecture for Reversible ALU based on ReversibleLogic

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Abstract-Programmable reversible logic is emerging as a prospective logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on circuit heat generation. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs. In this paper, the design reversible ALU based on different types of reversible gate used with minimal delay, and may be configured to produce a variety of logical calculations. The proposed reversible ALU based on DKG gates is verified and its advantages over the only existing adder design are quantitatively analyzed. The proposed design issynthesized using Xilinx ISE software and simulated using VHDL test bench.

Keywords—Reversible Gates, Reversible ALU based on PFAG Gate, Garbage Output, Quantum Cost.

I. INTRODUCTION

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n –input, n-output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. In this paper, we design a 16 bit reversible ALU that can perform eight operations simultaneously. The eight operations include addition, subtraction, AND, NAND, OR, NOR and XOR. All the modules are simulated in modalism SE 6.5 and synthesized using Xilinx ISE 14.1.

II. REVERSIBLE GATES

Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table shown in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

o BASIC REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available and is commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize various Boolean functions.

Several 4x4 gates have been described in the literature targeting low costand delay which may be implemented in a

programmable manner to produce high numberof logical calculations. The DKG gate produces the followinglogical output calculations:

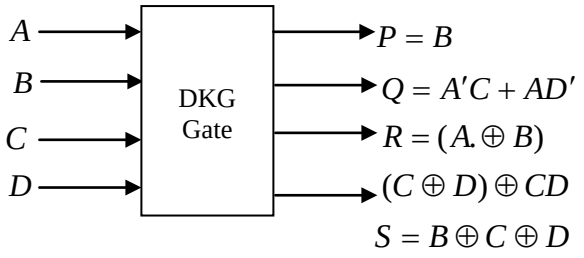

Figure 1: DKG Gate

$$P = B \quad (1)$$

$$Q = A'C + AD' \quad (2)$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \quad (3)$$

$$S = B \oplus C \oplus D \quad (4)$$

Table 1, shows the maximum path delay of all reversible logic gate with different types of device family. The basic principle of reversible computing is that a bijective device with the same variety of input and output lines can manufacture a computing setting wherever the electrodynamics of the system afford calculation of all future states supported noted past states, and also the system reaches each attainable state, leading to no temperature reduction. Reversible logic may be a logic method vogue during which there's a 1 to 1 mapping between the input and also the output vectors. BME is a 4*4 reversible gate whose block diagram is shown in fig.1.1. Having inputs (X,Y,Z,T) and outputs

P=X ', Q=XY xor Z , R=XT xor Z and S=X' Y xor Z xor T . Quantum cost of BME gate is 6.

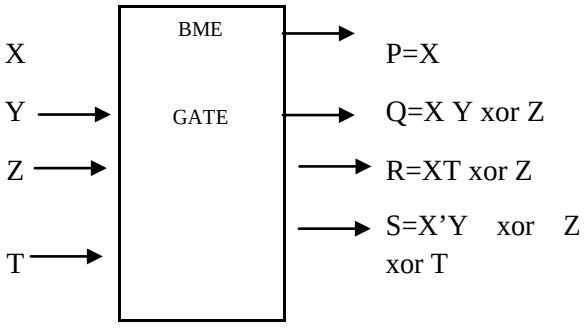

Figure. 1.1. Block Diagram of BME Gate

Table 1: Show maximum combination path delay of different reversible logic gate

Design	Virtex-4	Virtex-5	Virtex-6	Virtex-7
Feynman	4.858	3.696	0.832	0.803
Fredkin	4.936	3.813	0.918	0.905
Toffoli	4.949	3.809	0.918	0.905
Peres	4.949	3.813	0.981	0.905
MRG	4.987	3.881	0.989	0.953
TSG	4.989	3.881	0.984	0.948
PAOG	4.986	3.885	0.989	0.953
HNG	4.976	3.871	0.972	0.936
MKG	4.989	3.875	0.977	0.941
PFAG	4.976	3.871	0.972	0.936
DKG	4.987	3.881	0.984	0.948

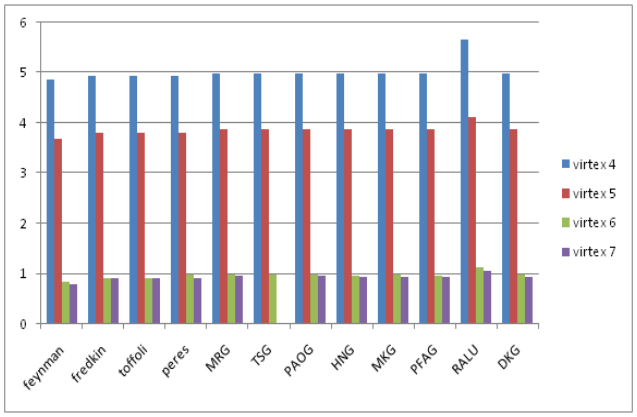

Figure 2: show delay of different reversible logic gate

III. PROPOSED DESIGN

The reversible ALU utilizes the DKG gate and **BME** gate to produce logical calculations: Adder and Sub tractor. The logical result depend on select line is shown in table 2. The proposed ALU based on DKG gates and existing design are shown in maximum combinational path delay table 2 to table 4 respectively

The binary full adder/sub tractor handles each input along with a carry in /borrow in that is generated as carry out/borrow out from the addition of previous lower order bits. If two n bit binary numbers are to be added or subtracted then n binary full adder/sub tractors should be cascaded. A parallel adder/sub tractor is the interconnection of a number of full adder/sub tractor and applying the inputs simultaneously.

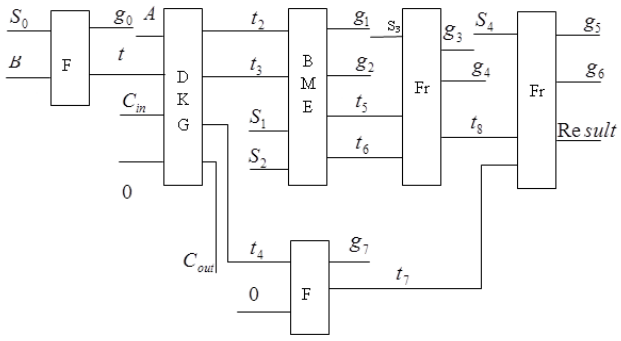

Figure 3: Block diagram of RALU based on DKG and BME

IV. SIMULATION RESULTS

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. The ISE 14.1i Design suite is accompanied by the release of chip scope Pro™ 14.1i debug and verification software. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-4 FX and Virtex-5 LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing. To simplify multi rate DSP and DHT designs with a large number of clocks typically found in wireless and video applications, ISE 14.1i software features breakthrough advancements in place and route and clock algorithm offering up to a 15 percent performance advantage. Xilinx 14.1i Provides the low memory requirement while providing expanded support for Microsoft windows Vista, Microsoft Windows XP x64, and Red Hat Enterprise WS 5.0 32-bit operating systems.

Table 2: Design RALU based on DKG Gate

	1-bit	2-bit	4-bit	8-bit	16-bit	32-bit
Vertex-4	5.997	6.207	7.684	8.899	16.328	21.911
Vertex-5	4.462	5.288	5.987	7.256	10.182	15.953
Vertex-6	1.494	1.847	2.432	3.603	5.943	10.623
Vertex-7	1.435	1.772	2.35	3.507	5.819	10.443

Table 3: Design RALU based on PFAG Gate

	1-bit	2-bit	4-bit	8-bit	16-bit	32-bit
Vertex -4	5.753	6.207	6.905	9.093	13.468	22.219
Vertex -5	4.129	4.987	5.509	6.955	9.436	15.657
Vertex -6	1.125	1.847	2.203	3.33	6.126	11.988
Vertex -7	1.062	1.772	2.11	3.238	5.944	11.656

S4	S3	S2	S1	S0	Cin	Result
0	0	0	0	0	0	Transfer A
0	0	0	0	0	1	Addition
1	0	1	0	0	0	Sub
1	0	0	0	0	1	XOR
0	1	0	0	0	0	OR
0	1	0	0	0	1	AND
1	1	0	0	0	0	NOT
1	1	0	1	0	1	NAND

Table 4: Design RALU based on TSG Gate

	1-bit	2-bit	4-bit	8-bit	16-bit	32-bit
Vertex -4	5.877	6.311	7.407	9.598	13.98	22.745
Vertex -5	5.109	5.502	6.197	7.587	10.366	15.926
Vertex -6	1.273	1.847	2.438	3.618	5.978	10.7
Vertex -7	1.226	1.772	2.356	3.522	5.854	10.52

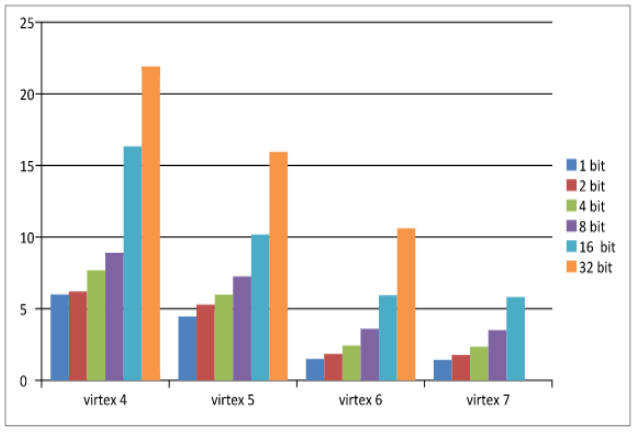

Figure 3: show delay of reversible ALU based on DKG logic gate

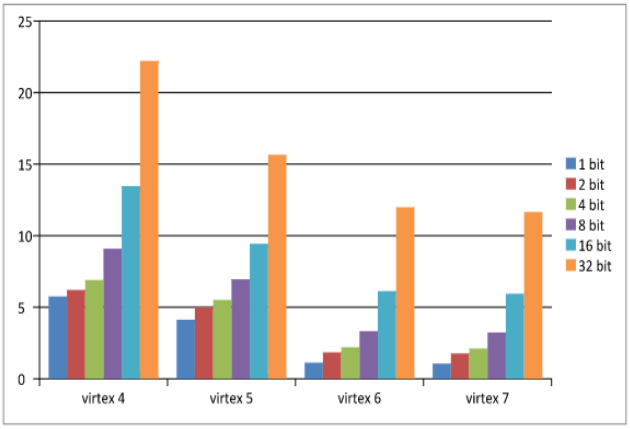

Figure 4: show delay of reversible ALU based on PFAG logic gate

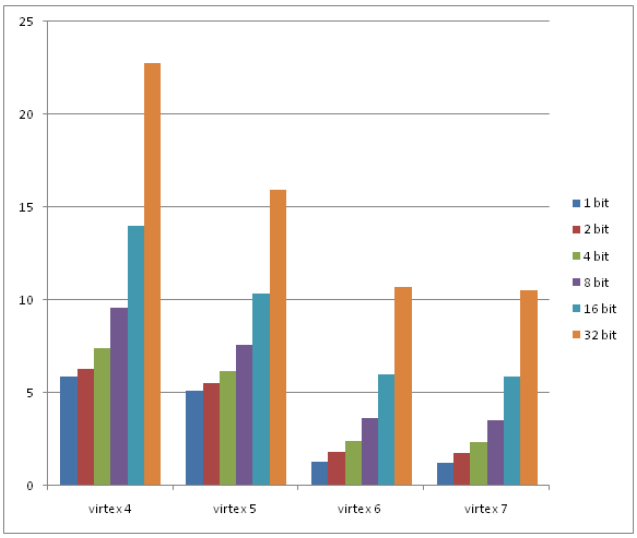

Figure 5: show delay of reversible ALU based on TSG logic gate

V. CONCLUSION

The 1-bit, 2-bit, 4-bit, 8-bit, 16-bit and 32bit reversible ALU is designed by integrating various sub modules that includes DKG logic Gate. The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

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